Aaron Myles Landwehr

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Summary

- Experienced in low-level firmware development and embedded hardware.
- Experienced in low-level software development and optimization.
- Familiarity with parallelizing algorithms for traditional shared memory, non-uniform memory access, and on distributed memory machines.
- Practical knowledge and experience working within teams
- Interested in learning new skills & acquiring new knowledge
- Ability to acquire new skills easily and efficiently

Skills

- Operating Systems: *BSD, Solaris, Linux/Unix, Windows
- Programming: C, C++, C#, Python, Java, Visual Basic, Assembly (RISC, X86), VHDL
- Parallel Architectures: GPU (CUDA, OpenCL), Cell, Cyclops64, Blue Gene/P, x86, Runnemede
- Runtime Technologies: POSIX Threads, Java Threads, OpenMP, MPI, OCR, Intel Concurrent Collections (CnC)
- Synthesis and Design: Vivado Design Suite, Xilinx Integrated Synthesis Environment
- Disassembly: Interactive Disassembler
- Project Management: CVS, SVN, HG (Mercurial), Git

Education

University of Delaware, Newark, DE

Fall 2016 – *Present*
Ph.D. in Electrical and Computer Engineering

University of Delaware, Newark, DE

Spring 2010 – *Summer 2016*
Masters of Science in Electrical and Computer Engineering

- Relevant Courses Taken Include:
  - Computer Networks
  - Sensor and Data Wireless Networks
  - PCB & FPGA Hardware Prototyping
  - Robotic Vision and Animal Behavior
  - Principles of Parallel Computer Architecture
  - Compiler Design
  - Advanced Compiler Design
  - Software Engineering
  - Object Oriented Software Engineering

University of Delaware, Newark, DE

Spring 2006 – 2010
Bachelor of Computer Engineering

- Relevant Courses Taken Include:
  - Object Oriented Programming with Java
  - Operating Systems
  - Data Structures
  - Field Theory
  - Random Signals and Noise
  - Digital Signal Processing
  - Physical Electronics
  - Introduction to VLSI Systems
  - High Performance Computing With commodity Hardware
  - Compiler Design
  - Computer Systems Design I & II
  - Introduction to Computer Systems Engineering
  - Microprocessor Systems
  - Introduction to Digital Systems

- Signals and Communication
- Electronic Circuit Analysis
- Analog Circuit Analysis

Delaware Technical and Community College, Newark, DE
Fall 2005
Accumulated credits toward an associate degree in Electrical Engineering
- Relevant Courses Taken Include:
  - Introduction to Programming
  - DC Circuit Analysis

Elkton High School, Elkton, MD
Completed in June 2005
- Earned High School Diploma.
- Multiple advanced placement courses taken.

Cecil College, North East, MD
Summer 2004
- Courses taken during high school career.

Experience

Research Assistant, CMOS VLSI Optimization Research Group (CVORG)
September 2016 – Present
- Implemented Vehicle-to-Grid (V2G) communication infrastructure to utilize aggregated vehicle statistics for decisions on whether to charge/discharge vehicles on the grid.
- Developed and maintained driving system software infrastructure for use with IRLED scene projection systems.
- Lead development of service based software infrastructure for running IRLED scene projection systems.
- Developed and maintained driving firmware for IRLED scene projection systems.
- Lead research and development of a novel Packaged Display Protocol (PDP) architecture for IRLED scene projection systems.

Research Assistant, Computer Architecture and Parallel Computer Laboratory (CAPSL)
September 2015 – March 2016
- Continued self-adaptive and introspective research efforts.
- Co-implemented an energy avoiding matrix multiplication algorithm utilizing energy efficient tiling on an experimental functional simulator modeling the Traleika Glacier many-core architecture created by Intel, Inc.
- Finished developed the Self-Aware Framework (SAFE) runtime to test and experiment with self-aware and self-adaptive control policies for temperature, energy, and power adaptation for future many-core architectures as part of Master's Thesis work.
- Investigated algorithms for reliability-aware runtime adaption via statically generated task scheduling.

Research Intern, ET International, Inc.
June 2015 – August 2015
- Benchmarked containment domain based resiliency within the dynamic adaptive SWARM runtime machine.
- Demonstrated containment domain based resiliency as an applicable extension to the codelet model of execution.

Research Assistant, Computer Architecture and Parallel Computer Laboratory (CAPSL)
September 2014 – May 2015
- Worked with FSim, an experimental functional simulator for modeling the Traleika Glacier many-core architecture as part of the X-Stack research initiative
- Continued development of the Self-Aware Framework (SAFE) runtime for energy and temperature management

Research Intern, Lawrence Livermore National Laboratory (LLNL)
Summer 2014

- Developed parallel molecular dynamics code using the Open Community Runtime (OCR)
- Studied the usability of OCR for certain classes of algorithms and data structures
- Examined and evaluated the constructs provided by various HPC programming models

Research Assistant, Computer Architecture and Parallel Computer Laboratory (CAPSL)
Fall 2010 – Spring 2014

- Self-adaptation and Introspection Research (November 2012 – 2014)
- Began development of a self-adaptive runtime system for energy and temperature management (2014)
- Implemented Parallelized LU Decomposition within Concurrent Collections (2012)
- Compiler Development for the Exascale Architectures (Mid 2011 – Early 2012)
- Involved in parallelization of a Turbulent Cloud Coalescence Simulation (– 2010)
- Optimizing FFT for Cyclops64 (Summer 2010)

Research Intern, Computer Architecture and Parallel Computer Laboratory (CAPSL)
December 2007 – 2010

- Involved in the parallelization of a Turbulent Cloud Coalescence Simulation (August 2009 –)
- Co-Developed a Distributed Shared Memory for BG/P using DCMF (May 2009 – August 2009)
- Co-Implemented a parallel FDTD algorithm for Cyclops64 (December 2008 – February 2009)
- Co-Implemented a parallel sorting algorithm for Cylcops64 (June 2008 – August 2008)
- Extensively modified a ray-tracer(Tachyon) for optimal performance on Cyclops64 (December 2007 – February 2008)

Developer for the Miranda-IM Project
Summer 2005 – 2007

- Worked with and analyzed TCP/IP Layer 5 Protocols
- Contributed and worked within a team oriented environment
- Solely Developed the AimOSCAR instant messenger protocol plugin for Miranda-IM
- Modified the AimTOC protocol plugin to support the TOC2 protocol
- Offered coding and debug assistance to other developers within the project
- Offered technical support to users of the Miranda-IM client

Publications

Toward a Packetized Display Protocol Architecture for IRLED Projector Systems
2018 IEEE Research and Applications of Photonics In Defense Conference (RAPID)

End to End Testing of IRLED Projectors
2018 IEEE Research and Applications of Photonics In Defense Conference (RAPID)

Gamma Correction and Operability of IRLED Scene Projectors
2018, Government Microcircuit Applications And Critical Technology Conference (GOMACTech)

Reliability-aware Runtime Adaptation Through a Statically Generated Task Schedule
2018, IEEE Transactions on Very Large Scale Integration (VLSI) Systems

Non-uniformity Correction (NUC) and 1Khz frame rate for IRLED Scene Projectors
2017, Government Microcircuit Applications And Critical Technology Conference (GOMACTech)

Test Plan for IRLED Scene Projectors
2017, Government Microcircuit Applications And Critical Technology Conference (GOMACTech)

An Experimental Exploration of Self-aware Systems for Exascale Architectures
2016 Master's Thesis

Resource Management for Running HPC Applications in Container Clouds
2016, International Conference on High Performance Computing (HiPC)

Energy Avoiding Matrix Multiply
2016, International Workshop on Languages and Compilers for Parallel Computing (LCPC)

A Landing Containment Domains on SWARM: Toward a Robust Resiliency Solution on a Dynamic Adaptive Runtime Machine
2015, The International Conference on Parallel Computing (ParCo)

Dynamic CPU Resource Allocation in Containerized Cloud Environments
2015, IEEE International Conference on Cluster Computing

Toward a Self-aware Codelet Execution Model
2014, Workshop on Data-Flow Execution Models for Extreme Scale Computing (DFM)

Toward a Self-aware System for Exascale Architectures
2013, European Conference on Parallel Processing (EuroPar)

Toward a Self-aware System for Exascale Architectures
2013, CAPSL Technical Memo 123

MACO: Metadata Coalescing and Optimizing Framework
2012, CAPSL Technical Memo 116

A Fresh Foundation for Software/Hardware Co-Design of Exascale Systems
2012, CAPSL Technical Memo 112

TiNy Threads on BlueGene/P: Exploring Many-Core Parallelisms Beyond the Traditional OS
2010, IEEE International Symposium on Parallel & Distributed Processing, Workshops and PhD. Forum (IPDPSW)

TiNy Threads on BlueGene/P: Exploring Many-Core Parallelisms Beyond the Traditional OS
2010, CAPSL Technical Memo 97